Design Project I

Vincent Luu and Kyle Powers

Lab Section 3:30PM – 6:00PM

"On our honor as students, we have not received nor given aid on this assignment"

Abstract

In Design Project I, a DC coupled multi-stage amplifier was designed, simulated, built, and experimentally verified. In the amplifier design, a transistor current source with a PNP input differential pair and an NPN common-base gain stage were used. For the specific values of the design, a code where the sum of the last digits of each partner's Social Security Number was used. From these given code values, resistor values had to be correctly chosen such that the circuit would operate in the given parameters. The following report contains our design approach for how we determined the values for our resistors and the correct AC midband gain for our amplifier; as well as, the calculated, measured, and simulated results for comparison.

Design Approach

First, the basic design values had to be derived from the code.

Code = (1/18) * (4 + 8) = **0.7** (rounded to the nearest tenth)

V_{CC} = ± (5 + 5 * Code) = **±8.5 V**

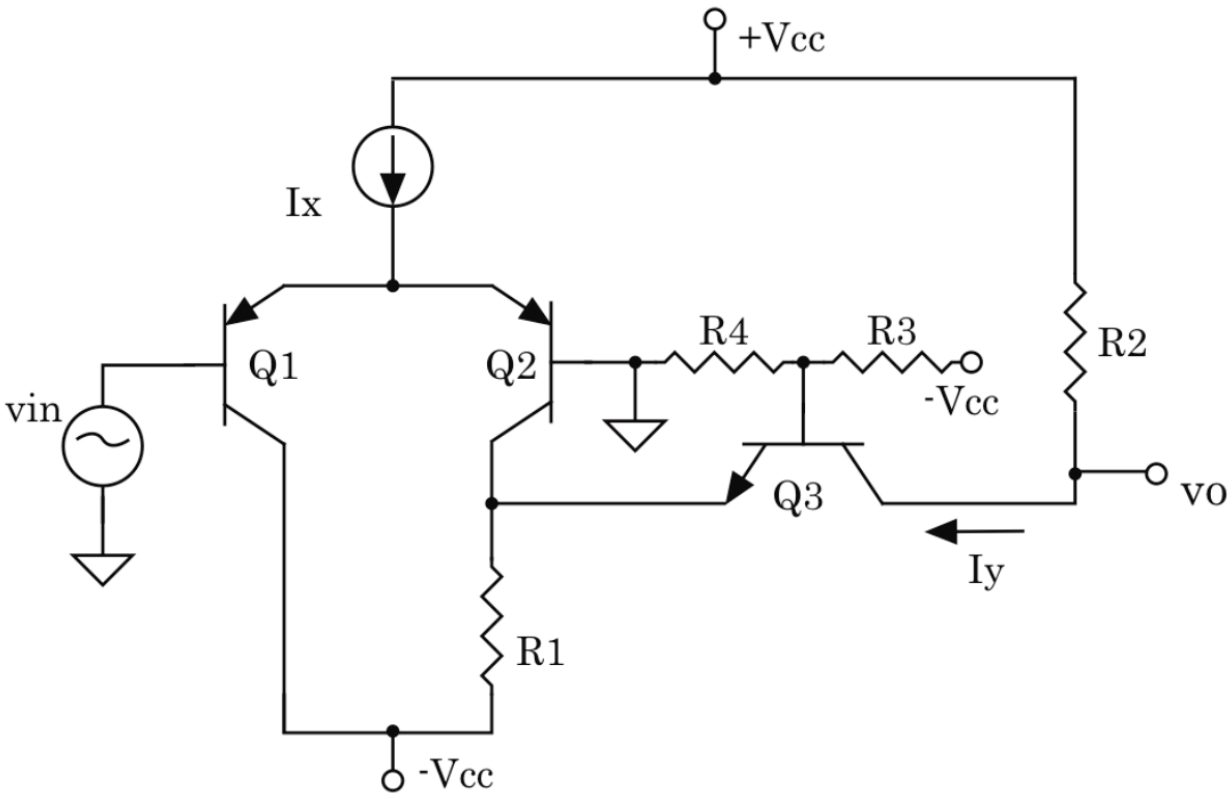
A_{mid} (v_o/v_{in}) = 25 * $|V_{CC}|$ = **212.5 V/V ± 10%**

$V_{out} \geq \pm (|V_{CC}| - 2)$ = **± 6.5 V**

I_X = 2 + Code = **2.7 mA**

$I_Y = I_X/2$ = **1.35 mA**

$|V_{OS}| \leq$ **± 0.4 V**



Defining Resistor Values

After the code-derived values, the values of the resistors were defined as:

$$R_1 = 370\ \Omega,\ R2 = 6300\ \Omega,\ R3 = 2000\ \Omega,\ R4 = 8000\ \Omega$$

The value of R_1 is dependent on the values of the voltage divider resistors (R_3 and R_4) because the value of V_{B3} determines the value of V_{E3}, in which case ohm's law can be used to solve for the value of R_1. Thus, a reasonable value was chosen in order to solve for R1. The value of R_2 is determined by setting V_{out} to 0V and then solving with ohm's law as well.

Increasing the AC Midband Gain

After all the values in the circuit had been solved for, hand calculations were used to determine the DC Bias and AC gains. In the end, the AC midband gain was found to be 159 V/V which was too low compared to the desired 212.5 V/V. In order to achieve the required gain, an active load was used in place of R_2. Also, a load resistor, R_L, was added. This caused the value of R_{C3}' to increase as the value of the load resistance increased which caused the third gain equation (v_O/v_{E3}) to increase as well. At this point, the value of R_L was increased to 9000 Ω. With the new gain value, the calculated AC midband gain turned out to be 227 V/V, which was in the range of 191 V/V to 233 V/V (212.5 V/V ± 10%).

Biasing the Transistor Current Source

The current source given in the topology had to be replaced with a transistor current source. By analyzing the circuit, biasing the transistor current source was required in order to achieve a higher voltage swing in the case of AC large signal analysis. With a lower value for R_5 and R_6, the active load resistance was lower and thus caused the voltage drop across R_2 to be lower. With R_2 lower, the V_O(MAX) for the AC large signal analysis would be higher.

Adjusting values to requirements

With the calculated results completed, the circuit was inputted in LTSpice and the DC Bias and AC analysis were simulated. The only adjustment that had to be made was changing R_1 because the output voltage had to be readjusted to be within the ± 0.4V range. Changing the value of R_1 slightly would be enough to get V_{out} close to 0V, so a potentiometer was placed in series with the R_1 resistor. The value of the R_1 resistor was determined by decreasing the value and then varied in 1 Ω steps by using the DC sweep function of LTSpice. The resulting resistance for R_1 was found to be 330 Ω. This was reconfirmed in lab where a potentiometer had been used to adjust the output voltage. The value found in lab for R_1 was 347 Ω. This could be due to the fact that the resistor values for other parts in the circuit were off slightly, but R_1 was still within reasonable range to the simulated value.

End Result Values

At the end of the design process the resistor values changed, mainly for R1 and R2. Also, a R_L value had to be included.

New Resistor Values: $R_1 = 330\ \Omega,\ R2 = 600\ \Omega,\ R3 = 2000\ \Omega,\ R4 = 8000\ \Omega,\ R_L = 9000\ \Omega$

Tables

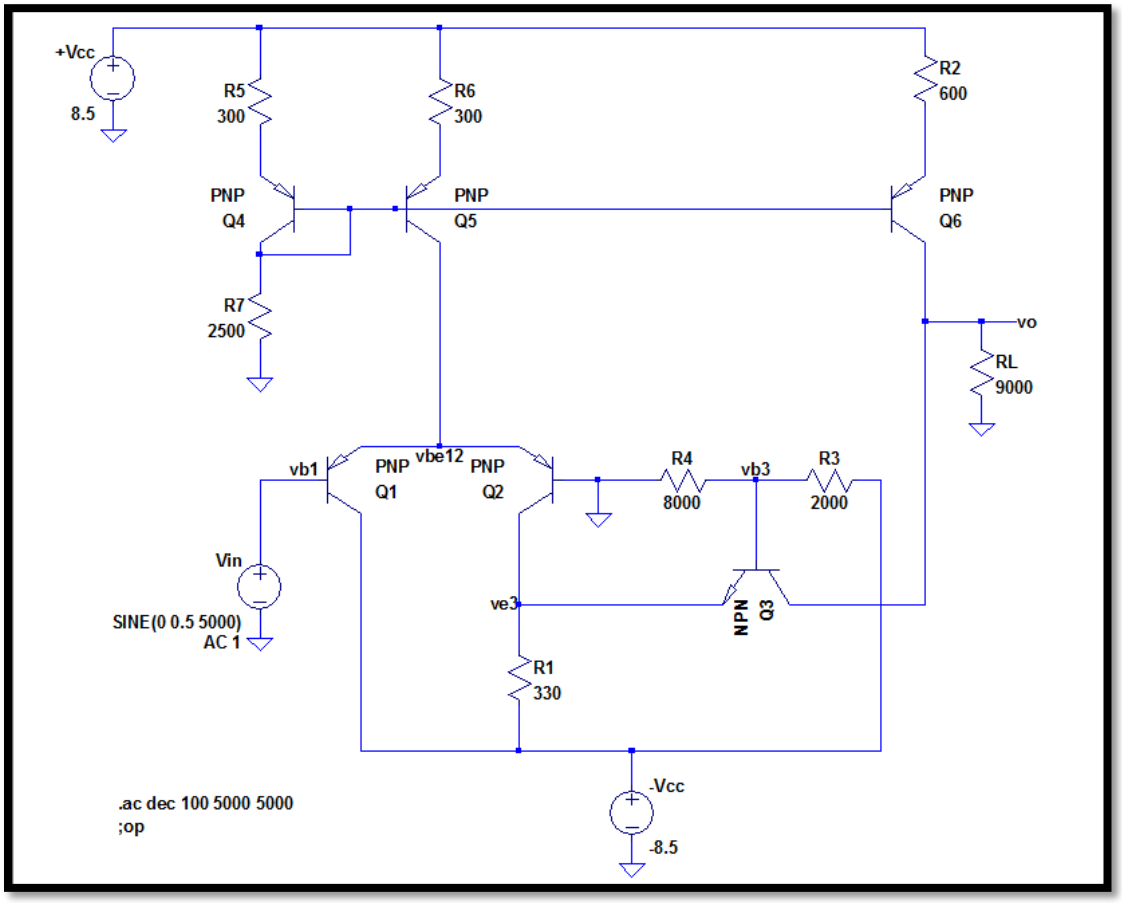
DC Bias			
	Calculated	**Measured**	**Simulated**
V_{B1}	0.00 V	0.005 V	0 V
V_{B3}	-6.80 V	-6.84 V	-6.82 V
V_{E3}	-7.50 V	-7.52 V	-7.60 V
V_{C3}	0.00 V	0.281 V	0.0164 V
I_X	2.70 mA	2.66 mA	2.69 mA
I_Y	1.35 mA	1.43 mA	1.37 mA

AC Midband Gain			
	Calculated	**Measured**	**Simulated**
$A(V_{B1}/V_{IN})$	1.00 V/V	0.978 V/V	1.00 V/V
$A(V_{E3}/V_{B1})$	0.668 V/V	0.621 V/V	0.604 V/V
$A(V_O/V_{E3})$	340 V/V	337 V/V	342 V/V
$A(V_O/V_{IN})$	227 V/V	209 V/V	207 V/V

Large Signal Transient Analysis			
	Calculated	**Measured**	**Simulated**
V_O(MAX)	6.99 V	7.30 V	7.64 V
V_O(MIN)	-6.80 V	-7.30 V	-7.64 V

AC Input/Output Impedance			
	Calculated	**Measured**	**Simulated**
R_{IN}	7.4 k Ω	37.0 k Ω	Ω
R_{OUT}	6.30 k Ω	3.19 k Ω	Ω

Final Circuit Design



LTSpice Results

--- Operating Point ---

V(Vcc):	8.5	voltage
V(-Vcc):	-8.5	voltage
V(vb1):	0	voltage
V(ve3):	-7.60431	voltage
V(vb3):	-6.82193	voltage
V(vo):	0.0163859	voltage
Ic(Q3):	0.00137034	device_current ← Iy
Ib(Q3):	1.37034e-005	device_current
Ie(Q3):	-0.00138405	device_current
Ic(Q6):	-0.00137216	device_current
Ib(Q6):	-1.37216e-005	device_current
Ie(Q6):	0.00138588	device_current
Ic(Q2):	-0.00133018	device_current
Ib(Q2):	-1.33018e-005	device_current
Ie(Q2):	0.00134348	device_current
Ic(Q1):	-0.00133018	device_current
Ib(Q1):	-1.33018e-005	device_current
Ie(Q1):	0.00134348	device_current
Ic(Q5):	-0.00268696	device_current ← Ix
Ib(Q5):	-2.68696e-005	device_current
Ie(Q5):	0.00271383	device_current
Ic(Q4):	-0.00268696	device_current
Ib(Q4):	-2.68696e-005	device_current
Ie(Q4):	0.00271383	device_current
I(Rl):	1.82065e-006	device_current
I(R2):	0.00138588	device_current
I(R1):	0.00271422	device_current
I(R3):	0.000839037	device_current
I(R4):	0.000852741	device_current
I(R6):	0.00271383	device_current
I(R7):	0.00275442	device_current
I(R5):	0.00271383	device_current

--- AC Analysis ---

frequency:	5000		Hz		
V(vb1):	mag:	1	phase:	0°	voltage
V(ve3):	mag:	0.603785	phase:	0°	voltage
V(vo):	mag:	207.43	phase:	0°	voltage

Conclusions

In this design project, a modified version of the given multi-stage amplifier had to be designed such that the AC midband gain had to be within a certain range based off a given code value. There were two big changes that had to be added to the design before the desired values could be achieved. First, an active load had to be added along with a load resistor to achieve a higher gain. Second, R_1 had to be adjusted with a potentiometer to ensure that the output voltage remained as close to 0V as possible. By changing around R1 and R2, the desired values could be achieved in order to design this multi-stage amplifier with the correct values based off the given code.