Kyle Powers
Assignment 3
Section 107
3/21/11

Introduction

The purpose of the laboratory assignment 3 was to design a simple sequential machine to provide a counter function. A written description of the problem was given. From there, a combinational logic circuit was designed to realize a function using D flip-flops and NAND gates.

Problem Statement

The problem in laboratory assignment 3 was to design a 3-bit synchronous counter that counts through a sequence that is shorter than the maximum possible. The counter would count through the following sequence: 111, 110, 100, 000, 001, 011, 111, 110... Asynchronous control inputs preset and clear were used to establish the desired initial state. Four flip=flops, and 2/3/4-input NAND gates were the only components that could be used.

Solution

The first step in solving the problem was to create a state chart, shown below.

	Present State	**Next State**
#	$Q_2\ Q_1\ Q_0$	$Q_2^+\ Q_1^+\ Q_0^+$
0	0 0 0	0 0 1
1	0 0 1	0 1 1
2	0 1 0	X X X
3	0 1 1	1 1 1
4	1 0 0	0 0 0
5	1 0 1	X X X
6	1 1 0	1 0 0
7	1 1 1	1 1 0

The second step was to create Karnaugh maps to realize Boolean equations and equivalences, as follows. Then, a logic circuit diagram was designed and tested in Logisim.

$D_2 = \sum m\ (3, 6, 7)$

$Q_2\ Q_1$	**00**	**01**	**11**	**10**
Q_0				
0	0	X	1	0
1	X	1	1	X

$D_2 = Q_1$

$D_1 = \sum m\ (1, 3, 7)$

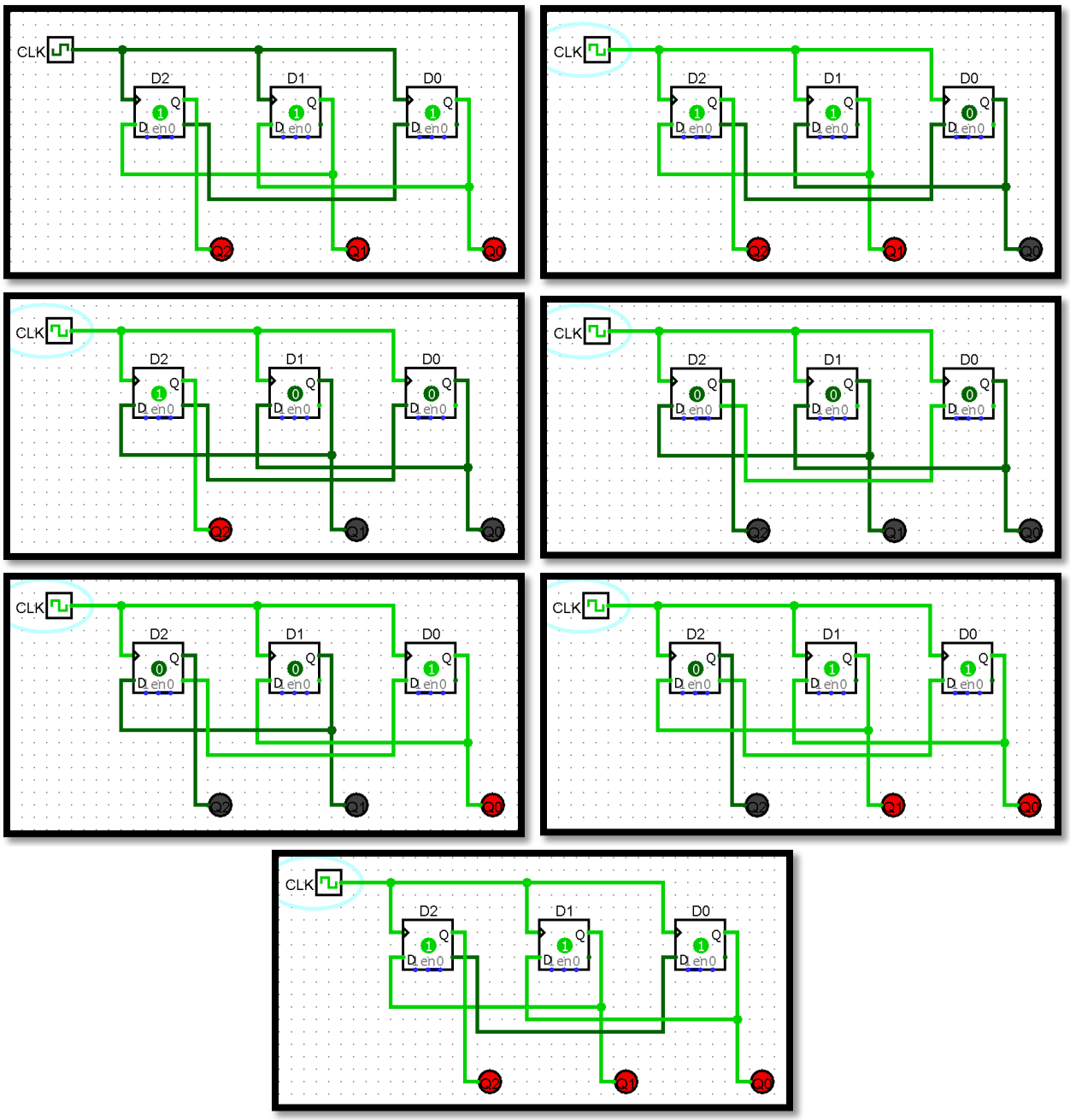
$Q_2\ Q_1$	**00**	**01**	**11**	**10**
Q_0				
0	0	X	0	0
1	1	1	1	X

$D_1 = Q_0$

$D_0 = \sum m\ (0, 1, 3)$

$Q_2\ Q_1$	00	01	11	10
Q_0				
0	1	X	0	0
1	0	1	1	X

$D_0 = Q_2'$



Problems Encountered

One problem encountered was how complicating the wiring became. This was resolved by starting over, slowly wiring from one point to another, while checking off its completion on my pre-laboratory diagram. Also, after an hour of troubleshooting, it was pointed out by the TA that my clock input was coming in from the wrong source. Once that was fixed, the circuit design was a success.

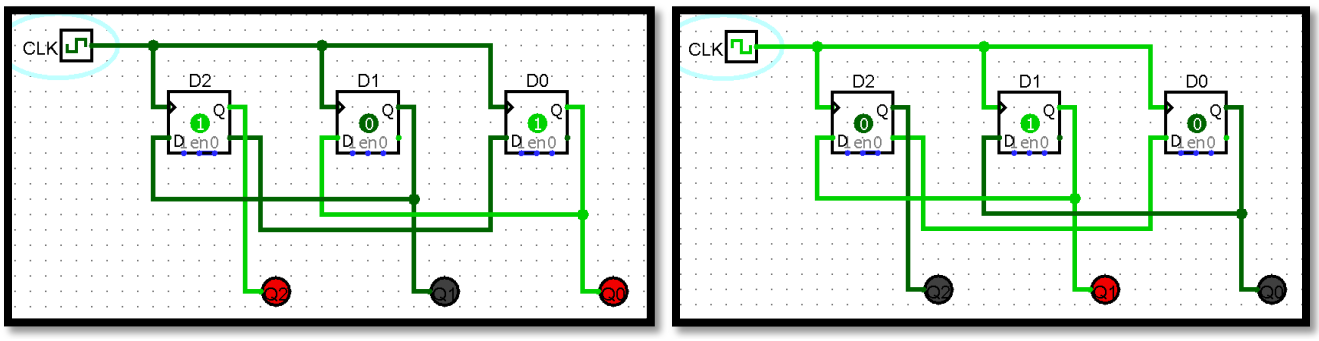
Conclusion

In the end, the sequential design for the counter was proven effective. While the laboratory assignment took about an hour and a half, due to the complications of wiring and the incorrect clock input, the use of Logisim to test the circuit diagram prior to lab proved to be an effective pre-laboratory decision. Laboratory assignment 3 ultimately enhanced my understanding of simple sequential machines.

Questions

1. Suppose that the initial state of your counter is 101. Use your flip-flop input functions to determine the count sequence that will result.

This results in a sequence of 101, 010, 101, 010…



2. A self-starting counter is one in which every possible state, even those not in the desired count sequence, has a sequence of transitions that eventually leads to a valid counter state. This guarantees that no matter how the counter starts up, it will eventually enter the proper counter sequence. Is your design a self starting counter? Justify your response.

If your counter is not a self-starting counter, how would you change your design to make it a self-starting counter?

No, my design is not a self-starting counter, because having the sequence begin at 101 or 010 results in an infinite loop of the series: 101, 01, 101, 01… The design would have to be altered so that when 101 or 010 is inputted, its output would resolve to either 111, 110, 100, 000, 001, or 011. Once the sequential circuit is at any of the outputs, the circuit will continue in its desired sequence. This is fairly easily accomplished by referring to the aforementioned Karnaugh maps and including all the X's (don't cares) in your function derivation. D_2 would become $Q_1 + Q_2Q_0$. D_1 would become $Q_0 + Q_2'Q_0'$. D_0 would become $Q2' + Q_1'Q_0$.

On my honor as a student of the University of Virginia, I have neither given nor received aid on this assignment.

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