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Assignment 5
Section 107
4/25/11

Introduction

The purpose of laboratory assignment 5 was to design a combinational data processing element. A written description of the problem was given. From there, the element would have both data and control inputs. Further, the element would be assembled from bit-wide cells.

Problem Statement

The problem in laboratory 5 was to design a combinational logic device that would take two n-bit positive binary numbers as input. An additional control bit was used to decide what operation the device would perform on the data words. The two possible operations would be addition and subtraction.

Solution

The first step was to complete the truth table for the combinational logic circuit.

a	**c_i**	**x**	**y**	**c_o**	**z**	**v**
0	0	0	0	0	1	0
0	0	0	1	0	0	0
0	0	1	0	1	0	1
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	1	1
0	1	1	0	1	1	0
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	1	0

The next step was to derive equations from the truth table:

3 data inputs: x, y, c_i

2 data outputs: z, c_o

1 control input: a

When a = 1, z = (x + y)

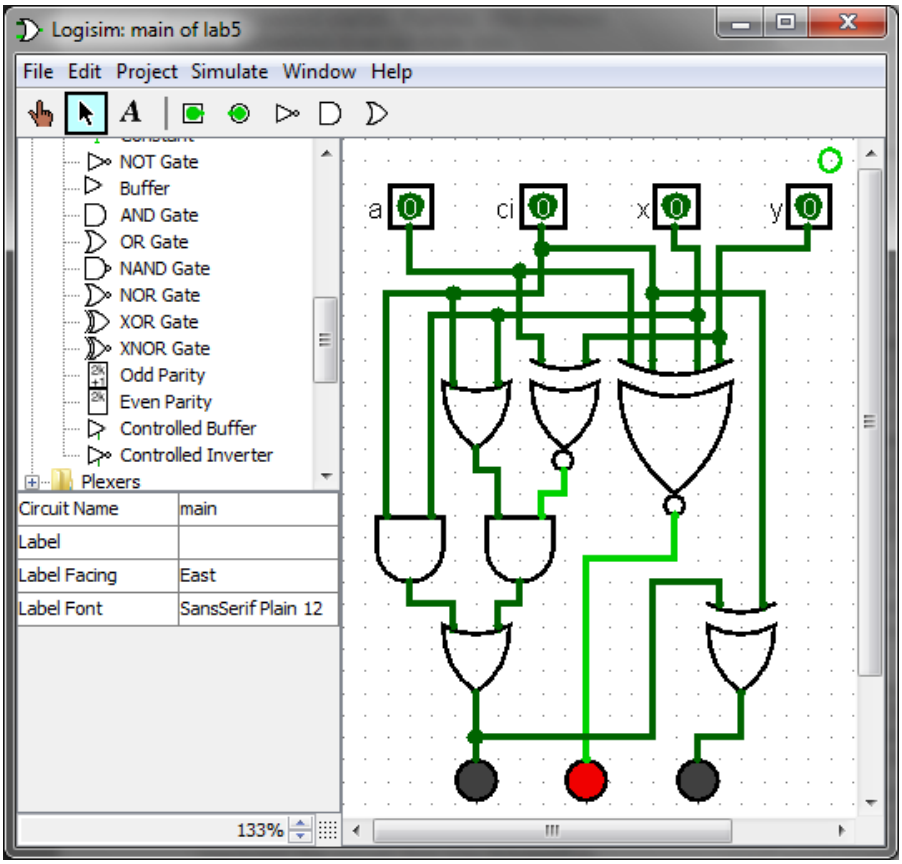
When a = 0, z = (x – y)

$$\mathbf{z = (x \oplus y \oplus a \oplus c_i)'}$$

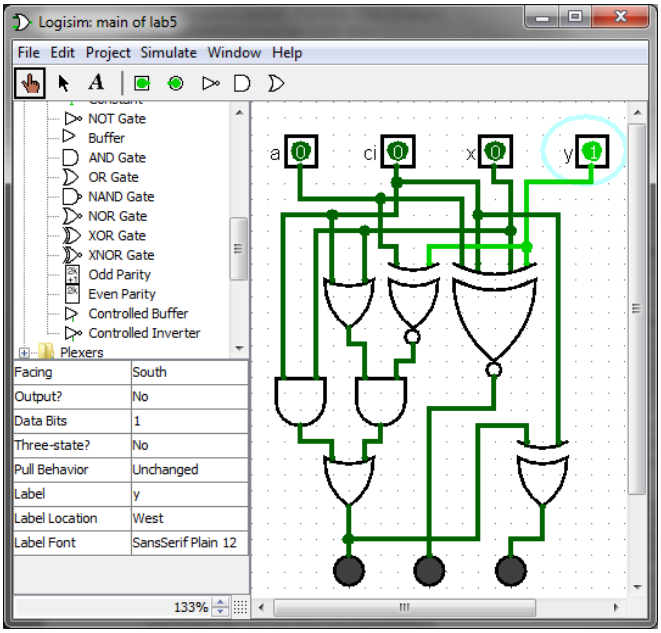
$$\mathbf{c_o = c_i x + (c_i + x)(a \oplus y)'}$$

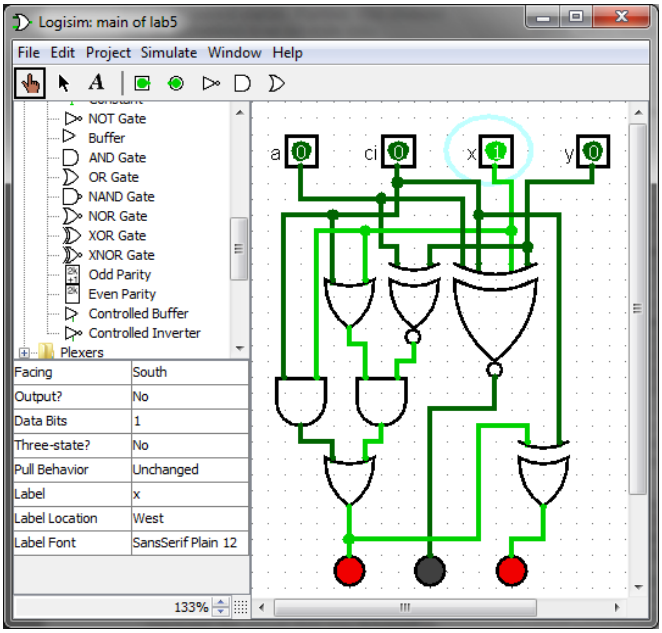
$$\mathbf{v = c_o \oplus c_i}$$

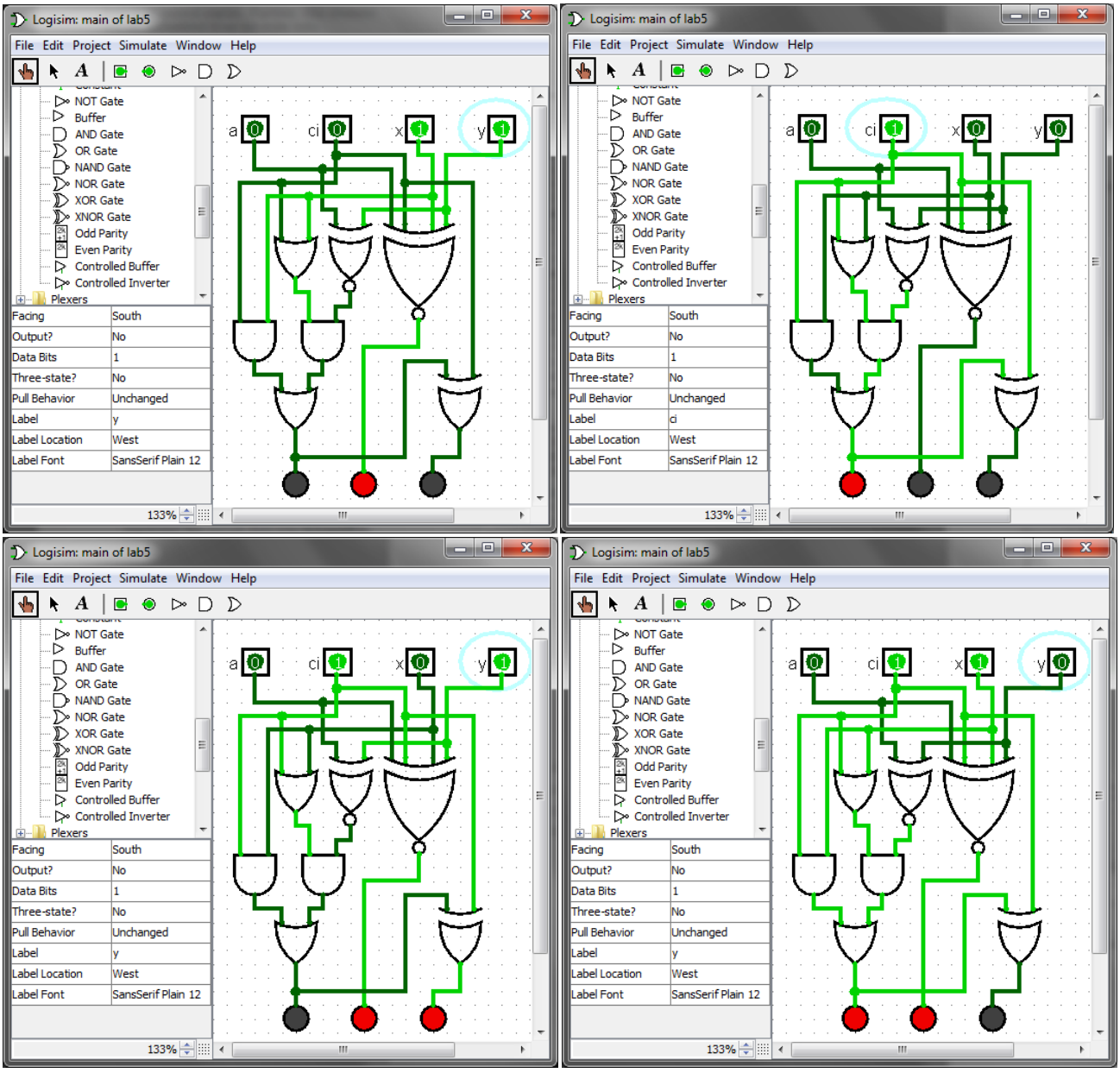
The next step was to turn the equations into logic circuits, which was done using Logisim:



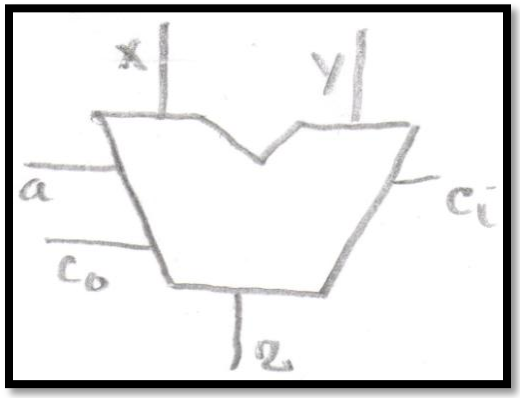
Follows are a few tests, demonstrating the correctness of the circuit design in regards to the truth table (the first LED from the left represents $\mathbf{c_o}$, the second represents **z**, and the third represents **v**):



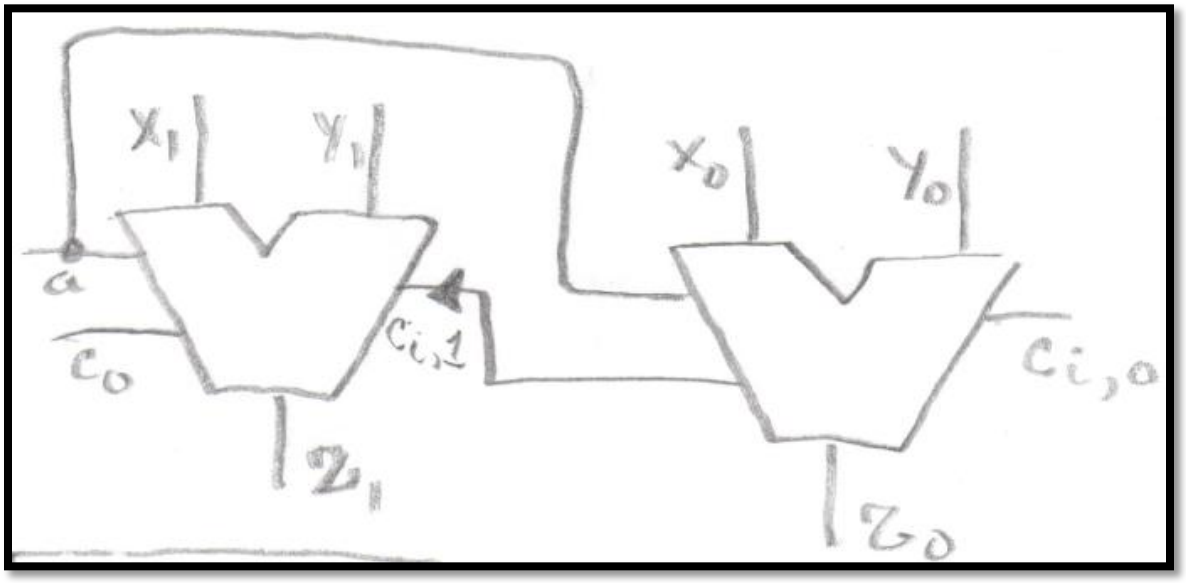




The next step was to use the symbol from the upper right of the lab assignment to represent the circuit that was just designed:



Afterwards, it was then necessary to draw a circuit that combined the aforementioned circuits into a 2-bit adder/subtractor – this was what was built in lab:



Problems Encountered

The only problem encountered was a faulty gate chip. This was diagnosed after an indicator LED continually flashed on and off, when it should have been continually on, in non-specific interval timings. Once the chip was simply replaced, the logic circuit worked flawlessly.

Conclusion

In the end, the design of a combinational data processing element was proven effective. While the laboratory assignment took less than hour to implement in lab – including the unfortunate occurrence of a faulty gate chip –, the use of Logisim to test the circuit diagram prior to lab proved to be an effective pre-laboratory decision. Laboratory 5 ultimately enhanced my understanding of combinational data processing elements.

On my honor as a student of the University of Virginia, I have neither given nor received aid on this assignment.

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